

IN THE CLAIMS:

1. (Once Amended) [A chip-like] An electronic component comprising at least one semiconductor chip having at least its electrodes formed exclusively on one surface thereof, and surfaces other than said one surface are continuously covered with a protective material.
2. (Once Amended) The [chip-like] electronic component according to claim 1 wherein said protective material comprises an organic insulating resin or an inorganic insulating material.
3. (Once Amended) The [chip-like] electronic component according to claim 1, comprising a semiconductor chip diced from a wafer at a position of said protective material for mounting on a package substrate, wherein said electrode is formed on said one surface, which is a device surface, of said semiconductor chip, and both a side wall and a bottom surface of said semiconductor chip are covered with said protective material.
4. (Once Amended) The [chip-like] electronic component according to claim 3 wherein a solder bump is formed on said electrode.
5. (Once Amended) The [chip-like] electronic component according to claim 1 wherein a [plurality and/or a] plurality of different types of semiconductor chips are integrated [as] and bonded by said protective material.
6. (Once Amended) A pseudo wafer comprising a plurality [and/or a plurality] of [different types of chip-like electronic components] semiconductor chips each having at least their electrodes formed solely on one surface thereof, wherein interspaces between said

plurality and/or said [plurality of different types of chip-like electronic components] chips and bottom surfaces thereof are continuously covered with said protective material, and the chips are bonded with each other.

8. (Once Amended) The pseudo wafer according to claim 6 wherein said plurality [and/or said plurality] of [different types of] semiconductor chips arrayed thereon are diced at a position of said protective material between said plurality of semiconductor chips and [fabricated into a discrete chip or an integrated semiconductor chip integrating a plurality and/or a plurality of different types of semiconductor chips to be] thereafter mounted on a packaging substrate.

REMARKS

Applicants thank the Examiner for acknowledging receipt of Applicants' foreign priority documents that have been submitted pursuant to 35 U.S.C. §119. Applicants have submitted a drawing amendment pursuant to the Examiner's request. Applicants request entry of these proposed changes. Applicants also have amended the specification to make the appropriate reference to Figures 5A – 5J and have modified page 25 line 1 to remove a minor typographical error.

Applicants respectfully request reconsideration of the Examiner's rejections that have been set forth under 35 U.S.C. §112, second paragraph. Applicants have amended the claims in order to overcome these rejections. Applicants submit that the amended claims comport with all the requirements of §112. Accordingly, Applicants request that the Examiner now withdraw these rejections.

Applicants respectfully request reconsideration of the prior art rejections set forth by the Examiner under 35 U.S.C. §§102 and 103. Applicants submit that the prior art references